AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated in the following listing of all claims:

1. (Currently Amended) An integrated circuit receiving command information over a plurality of bit times, comprising:

a command queue storing command information received into the integrated circuit during consecutive bit times; and

control logic responsive to a cancellation indication in the command information, indicating that a command is canceled, to repoint a write pointer to point to the canceled command already stored in the command queue; and

wherein the command queue includes a plurality of FIFO buffers, each of the FIFO buffers storing a segment of a received command and wherein a plurality of write pointers point to locations in respective FIFO buffers to store a next command segment, and wherein segments of a command in different FIFO buffers are received at different bit times.

2. (Original) The integrated circuit as recited in claim 1 wherein the command is a speculative read operation.

3. (Cancelled)

4. (Currently Amended) The integrated circuit as recited in ~~claim 3~~ claim 1 wherein a last FIFO storing a last command segment received during a last bit time for the command information is written to store a last portion of the command.

5. (Original) The integrated circuit as recited in claim 4 wherein the indication to cancel the current command is in the last command segment.

6. (Original) The integrated circuit as recited in claim 4 wherein each of the plurality of FIFOs has its respective write pointer decremented in consecutive clock intervals.

7. (Original) The integrated circuit as recited in claim 1 further comprising a content counter indicating a number of commands stored in the command buffer.

8. (Original) The integrated circuit as recited in claim 7 wherein the content counter is decremented as a result of the cancellation indication.

9. (Currently Amended) A method for storing command information into a command queue in an integrated circuit, comprising:

receiving a plurality of command segments corresponding to one command in a plurality of phases, each command segment being received in a different phase;

pushing received command segments into a command queue;

checking for a cancellation indication for the command being received;

in response to the cancellation indication, performing an undo-push operation to remove the command segments stored in the command queue associated with the cancelled command; and

wherein the command queue includes a plurality of FIFO buffers, each of the FIFO buffers storing respective command segments of a command received in a different bit time and wherein a plurality of write pointers point to locations in respective FIFO buffers to store a next command segment.

10. (Cancelled)

11. (Currently Amended) The method as recited in ~~claim 10~~ claim 9 wherein the undo push operation includes decrementing the plurality of write pointers.

12. (Original) The method as recited in claim 9 wherein further comprising writing a last command segment into a last FIFO buffer, the last command segment including the cancellation indication.

13. (Original) The method as recited in claim 9 wherein the cancelled command is a speculative read command.

14. (Original) The method as recited in claim 13 wherein the cancellation indication is a read valid bit indicating that the speculative read command is not valid.

15. (Currently Amended) The method as recited in ~~claim 10~~ claim 9 wherein the plurality of write pointers are decremented consecutively.

16. (Original) The method as recited in claim 15 wherein the undo push operation is started within one clock of receipt of the cancellation indication.

17. (Original) The method as recited in claim 9 further comprising maintaining a count of a number of commands currently in the command buffer.

18. (Original) The method as recited in claim 17 further comprising decrementing the count in response to the cancellation indication.

19. (Currently amended) A computer system comprising:

a processor;

an integrated circuit coupled to receive a command from the processor over a command channel, the command being received in command segments at corresponding different times;

a command queue in the integrated circuit coupled to receive the command segments, wherein the command queue includes a plurality of FIFO buffers, each of the FIFO buffers storing respective command segments of a command received in a different bit time and wherein a plurality of write pointers point to locations in respective FIFO buffers to store a next command segment; and

control logic coupled the command queue and responsive to a cancellation indication in one of the command segments indicative that a current command is canceled to perform an undo-push operation such that a next received command is placed in the command queue in a same location as the current command.

20. (Original) The computer system as recited in claim 19 wherein the integrated circuit includes a count of a number of commands in the command queue and wherein the count is decremented in response to the cancellation indication.